

# 1-Mbit (128K x 8) Static RAM

## Features

- **Temperature Ranges**
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
  - Automotive-A: -40°C to 85°C
  - Automotive-E: -40°C to 125°C
- **4.5V–5.5V operation**
- **CMOS for optimum speed/power**
- **Low active power**  
(70 ns Commercial, Industrial, Automotive-A)
  - 82.5 mW (max.) (15 mA)
- **Low standby power**  
(55/70 ns Commercial, Industrial, Automotive-A)
  - 110 μW (max.) (15 μA)
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  options**
- **Available in Pb-free and non-Pb-free 32-pin (450 mil-wide) SOIC, 32-pin STSOP and 32-pin TSOP-I**

## Functional Description<sup>[1]</sup>

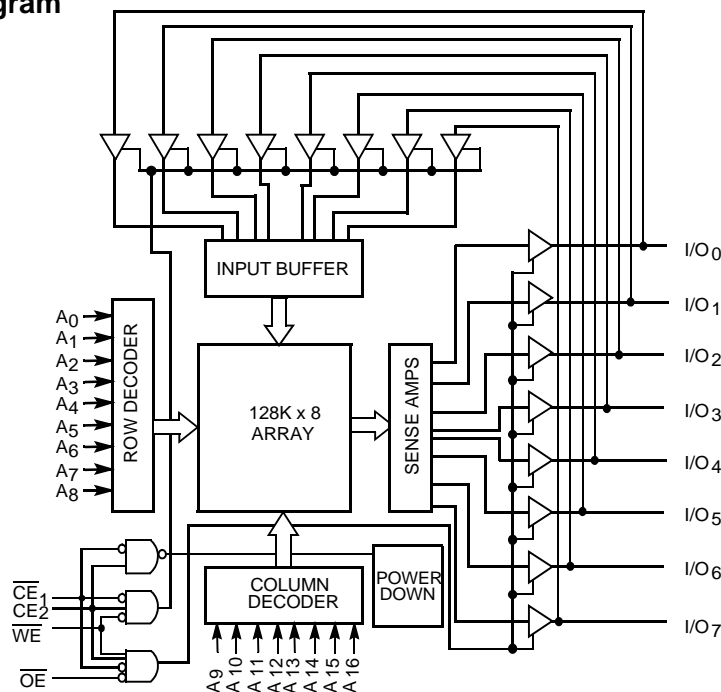
The CY62128BN is a high-performance CMOS static RAM organized as 128K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}_1$ ), an active HIGH Chip Enable ( $CE_2$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking Chip Enable One ( $\overline{CE}_1$ ) and Write Enable (WE) inputs LOW and Chip Enable Two ( $CE_2$ ) input HIGH. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

Reading from the device is accomplished by taking Chip Enable One ( $\overline{CE}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable (WE) and Chip Enable Two ( $CE_2$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

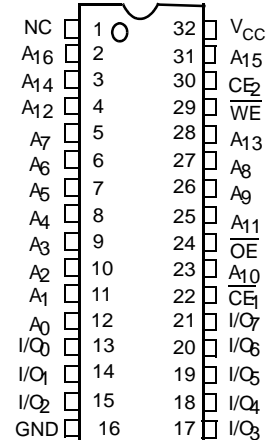
The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and WE LOW).

## Logic Block Diagram



## Pin Configuration

### Top View SOIC



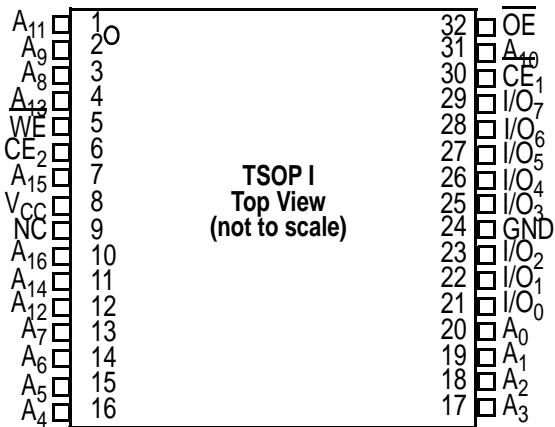
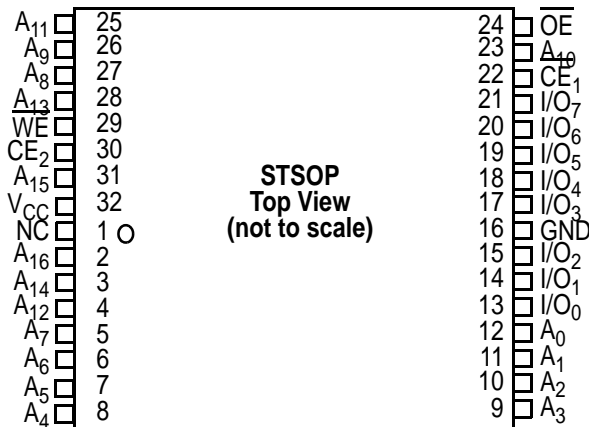
### Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Product Portfolio**

Product		V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation			
						Operating, I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (μA)	
		Min.	Typ. <sup>[2]</sup>	Max.		Typ. <sup>[2]</sup>	Max.	Typ. <sup>[2]</sup>	Max.
CY62128BNLL	Commercial	4.5	5.0	5.5	55	7.5	20	2.5	15
					70	6	15	2.5	15
	Industrial				55	7.5	20	2.5	15
					70	6	15	2.5	15
	Automotive-A				70	6	15	2.5	15
	Automotive-E				70	6	25	2.5	25

**Pin Configurations**



**Pin Definitions**

Input	A <sub>0</sub> –A <sub>16</sub> . Address Inputs
Input/Output	I/O <sub>0</sub> –I/O <sub>7</sub> . Data lines. Used as input or output lines depending on operation
Input/Control	WE. Write Enable, Active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
Input/Control	CE <sub>1</sub> . Chip Enable 1, Active LOW.
Input/Control	CE <sub>2</sub> . Chip Enable 2, Active HIGH.
Input/Control	OE. Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins
Ground	GND. Ground for the device
Power Supply	V <sub>CC</sub> . Power supply for the device

**Note:**

2. Typical values are included for reference only and are not tested or guaranteed. Typical values are an average of the distribution across normal production variations as measured at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25 °C, and t<sub>AA</sub> = 70 ns.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature .....-65°C to +150°C
- Ambient Temperature with Power Applied.....-55°C to +125°C
- Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[3]</sup> .... -0.5V to +7.0V
- DC Voltage Applied to Outputs in High-Z State<sup>[3]</sup> .....-0.5V to V<sub>CC</sub> + 0.5V
- DC Input Voltage<sup>[3]</sup>.....-0.5V to V<sub>CC</sub> + 0.5V
- Current into Outputs (LOW) .....20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

**Operating Range**

Range	Ambient Temperature (T <sub>A</sub> ) <sup>[4]</sup>	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	
Automotive-A	-40°C to +85°C	
Automotive-E	-40°C to +125°C	

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	-55			-70			Unit	
			Min.	Typ. <sup>[2]</sup>	Max.	Min.	Typ. <sup>[2]</sup>	Max.		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.4			2.4			V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.1 mA			0.4			0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.2		V <sub>CC</sub> + 0.3	2.2		V <sub>CC</sub> + 0.3	V	
V <sub>IL</sub>	Input LOW Voltage <sup>[3]</sup>		-0.3		0.8	-0.3		0.8	V	
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Commercial/Industrial	-1		+1	-1		+1	μA
			Automotive-A				-1		+1	μA
			Automotive-E				-10		+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	Commercial/Industrial	-1		+1	-1		+1	μA
			Automotive-A				-1		+1	μA
			Automotive-E				-10		+10	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Commercial/Industrial		7.5	20		6	15	mA
			Automotive-A					6	15	mA
			Automotive-E					6	25	mA
I <sub>SB1</sub>	Automatic CE Power-down Current —TTL Inputs	Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>IH</sub> or CE <sub>2</sub> ≤ V <sub>IL</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Commercial/Industrial		0.1	2		0.1	1	mA
			Automotive-A					0.1	1	mA
			Automotive-E					0.1	2	mA
I <sub>SB2</sub>	Automatic CE Power-down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V, or CE <sub>2</sub> ≤ 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	Commercial/Industrial		2.5	15		2.5	15	μA
			Automotive-A					2.5	15	μA
			Automotive-E					2.5	25	μA

**Notes:**

- 3. V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- 4. T<sub>A</sub> is the "Instant On" case temperature.

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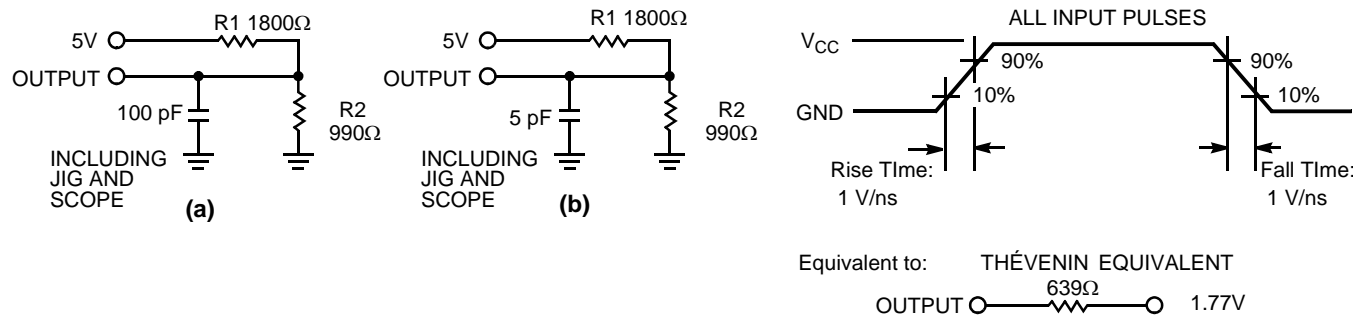
**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	9	pF
C <sub>OUT</sub>	Output Capacitance		9	pF

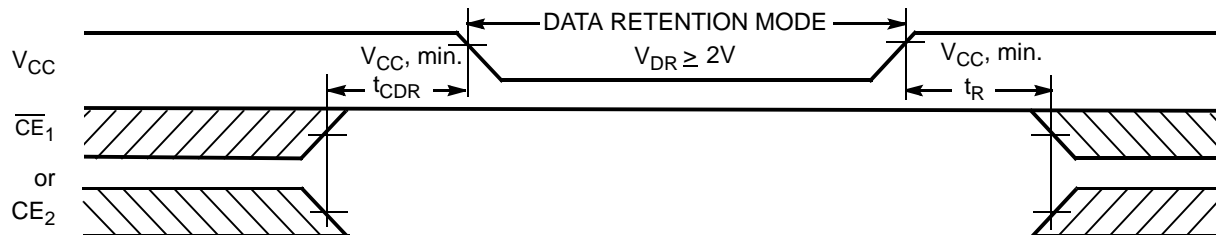
**Thermal Resistance<sup>[5]</sup>**

Parameter	Description	Test Conditions	32 SOIC	32 STSOP	32 TSOP	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	66.17	105.14	97.44	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		30.87	14.09	26.05	°C/W

**AC Test Loads and Waveforms**



**Data Retention Waveform**



**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions <sup>[6]</sup>	Min.	Typ.	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		2.0			V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = V <sub>DR</sub> = 2.0V, CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V, or CE <sub>2</sub> ≤ 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or, V <sub>IN</sub> ≤ 0.3V	Commercial/ Industrial Automotive-A	1.5	15	μA
			Automotive-E	1.5	25	μA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub>	Operation Recovery Time		70			ns

**Note:**

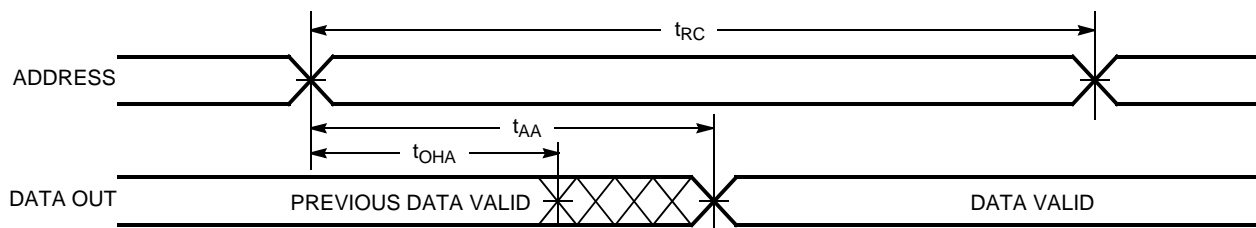
- 5. Tested initially and after any design or process changes that may affect these parameters.
- 6. No input may exceed V<sub>CC</sub> + 0.5V.

**Switching Characteristics<sup>[7]</sup> Over the Operating Range**

Parameter	Description	CY62128BN-55		CY62128BN-70		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
$t_{RC}$	Read Cycle Time	55		70		ns
$t_{AA}$	Address to Data Valid		55		70	ns
$t_{OHA}$	Data Hold from Address Change	5		5		ns
$t_{ACE}$	$\overline{CE}_1$ LOW to Data Valid, $CE_2$ HIGH to Data Valid		55		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		20		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[7, 9]</sup>		20		25	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW to Low Z, $CE_2$ HIGH to Low Z <sup>[9]</sup>	5		5		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH to High Z, $CE_2$ LOW to High Z <sup>[8, 9]</sup>		20		25	ns
$t_{PU}$	$\overline{CE}_1$ LOW to Power-up, $CE_2$ HIGH to Power-up	0		0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH to Power-down, $CE_2$ LOW to Power-down		55		70	ns
<b>WRITE CYCLE<sup>[10]</sup></b>						
$t_{WC}$	Write Cycle Time	55		70		ns
$t_{SCE}$	$\overline{CE}_1$ LOW to Write End, $CE_2$ HIGH to Write End	45		60		ns
$t_{AW}$	Address Set-up to Write End	45		60		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	45		50		ns
$t_{SD}$	Data Set-up to Write End	25		30		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[9]</sup>	5		5		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[8, 9]</sup>		20		25	ns

**Switching Waveforms**

**Read Cycle No.1<sup>[11, 12]</sup>**



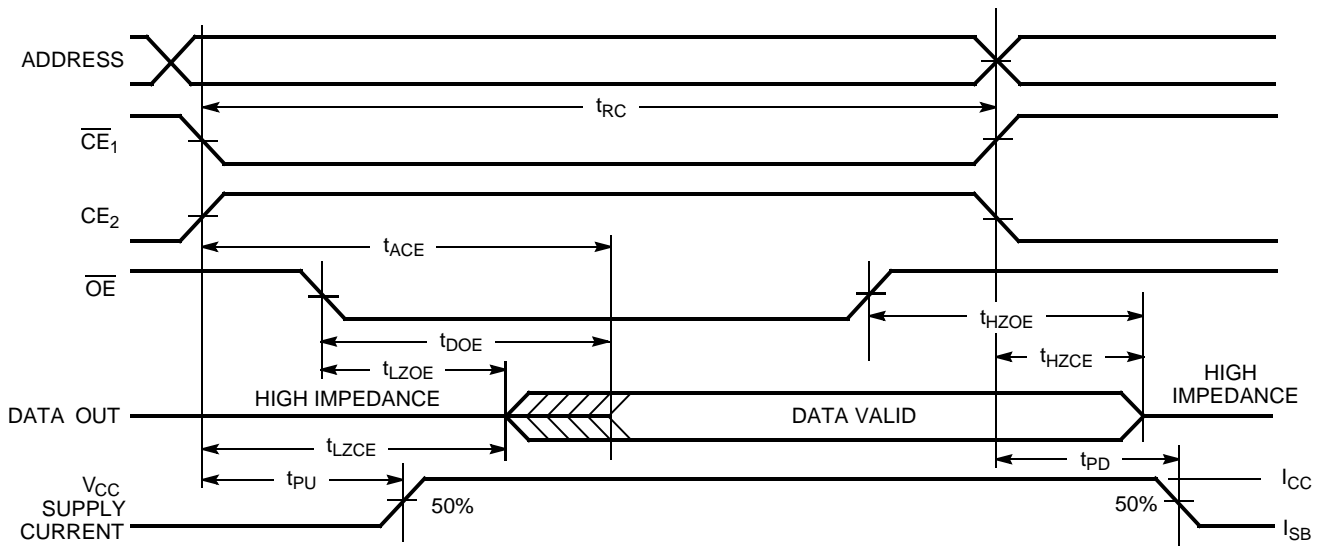
**Notes:**

7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 100-pF load capacitance.
8.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
9. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
10. The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW and  $CE_2$  HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
12.  $\overline{WE}$  is HIGH for read cycle.

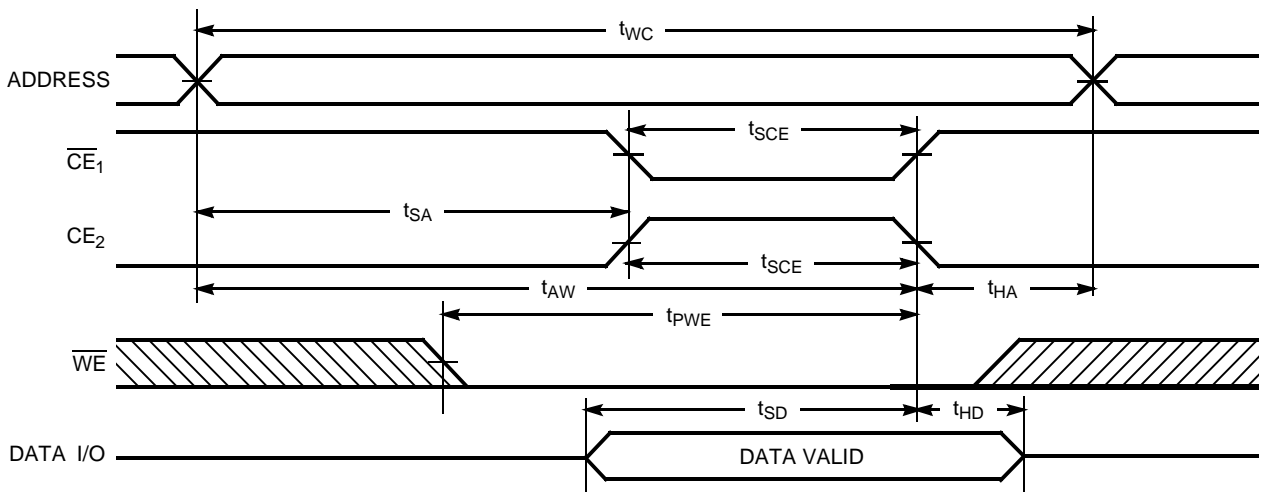
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Switching Waveforms (continued)

Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[12, 13]</sup>



Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled)<sup>[14, 15]</sup>



Notes:

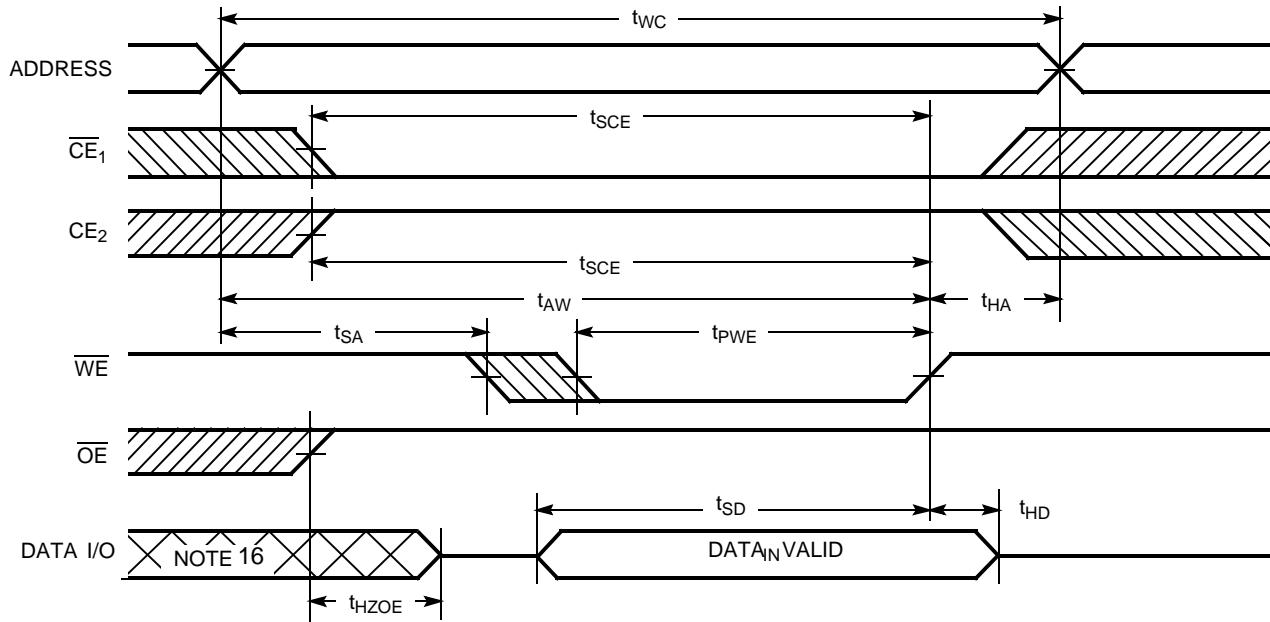
- 13. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.
- 14. Data I/O is high impedance if  $OE = V_{IH}$ .
- 15. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

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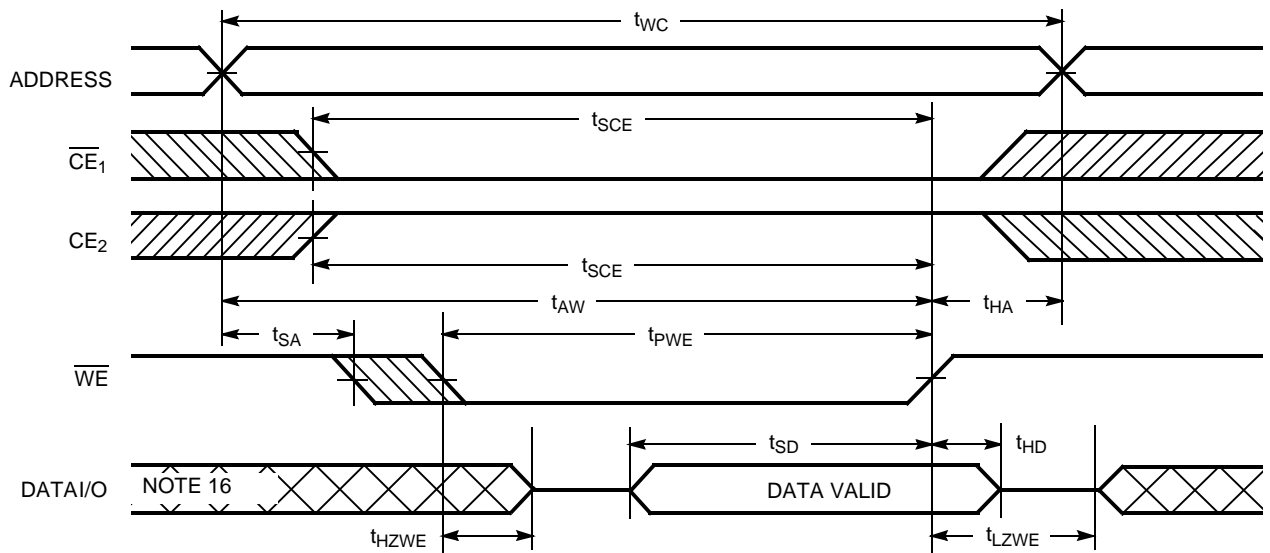


Switching Waveforms (continued)

Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[14, 15]</sup>



Write Cycle No.3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[14, 15]</sup>



**Note:**  
16. During this period the I/Os are in the output state and input signals should not be applied.

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**Truth Table**

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	X	High Z	Power-down	Standby (I <sub>SB</sub> )
X	L	X	X	High Z	Power-down	Standby (I <sub>SB</sub> )
L	H	L	H	Data Out	Read	Active (I <sub>CC</sub> )
L	H	X	L	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62128BNLL-55SC	51-85081	32-pin 450-Mil SOIC	Commercial
	CY62128BNLL-55SXC		32-pin 450-Mil SOIC (Pb-Free)	
	CY62128BNLL-55SI		32-pin 450-Mil SOIC	Industrial
	CY62128BNLL-55SXI		32-pin 450-Mil SOIC (Pb-Free)	
	CY62128BNLL-55ZAI	51-85094	32-pin STSOP	
	CY62128BNLL-55ZAXI	32-pin STSOP (Pb-Free)		
	CY62128BNLL-55ZI	51-85056	32-pin TSOP Type I	
	CY62128BNLL-55ZXI		32-pin TSOP Type I (Pb-Free)	
70	CY62128BNLL-70SC	51-85081	32-pin 450-Mil SOIC	Commercial
	CY62128BNLL-70SXC		32-pin 450-Mil SOIC (Pb-Free)	
	CY62128BNLL-70ZC	51-85056	32-pin TSOP Type I	
	CY62128BNLL-70ZXC		32-pin TSOP Type I (Pb-Free)	
	CY62128BNLL-70SI	51-85081	32-pin 450-Mil SOIC	Industrial
	CY62128BNLL-70SXI		32-pin 450-Mil SOIC (Pb-Free)	
	CY62128BNLL-70ZAI	51-85094	32-pin STSOP	
	CY62128BNLL-70ZAXI		32-pin STSOP (Pb-Free)	
	CY62128BNLL-70ZI	51-85056	32-pin TSOP Type I	
	CY62128BNLL-70ZXI		32-pin TSOP Type I (Pb-Free)	
	CY62128BNLL-70ZXA	51-85056	32-pin TSOP Type I (Pb-Free)	Automotive-A
	CY62128BNLL-70SXA	51-85081	32-pin 450-Mil SOIC (Pb-Free)	
	CY62128BNLL-70SXE	51-85081	32-pin 450-Mil SOIC (Pb-Free)	Automotive-E
	CY62128BNLL-70ZAXE	51-85094	32-pin STSOP (Pb-Free)	

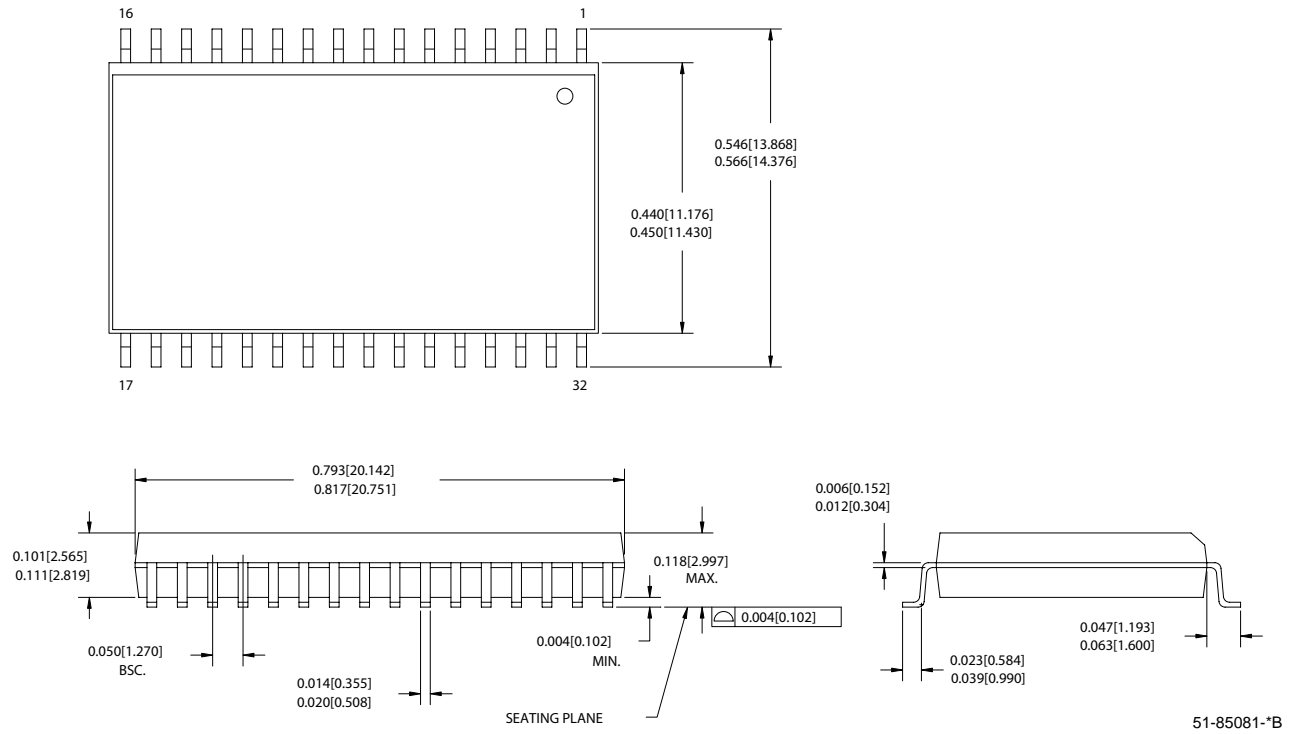
Please contact your local Cypress sales representative for availability of these parts

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Package Diagrams

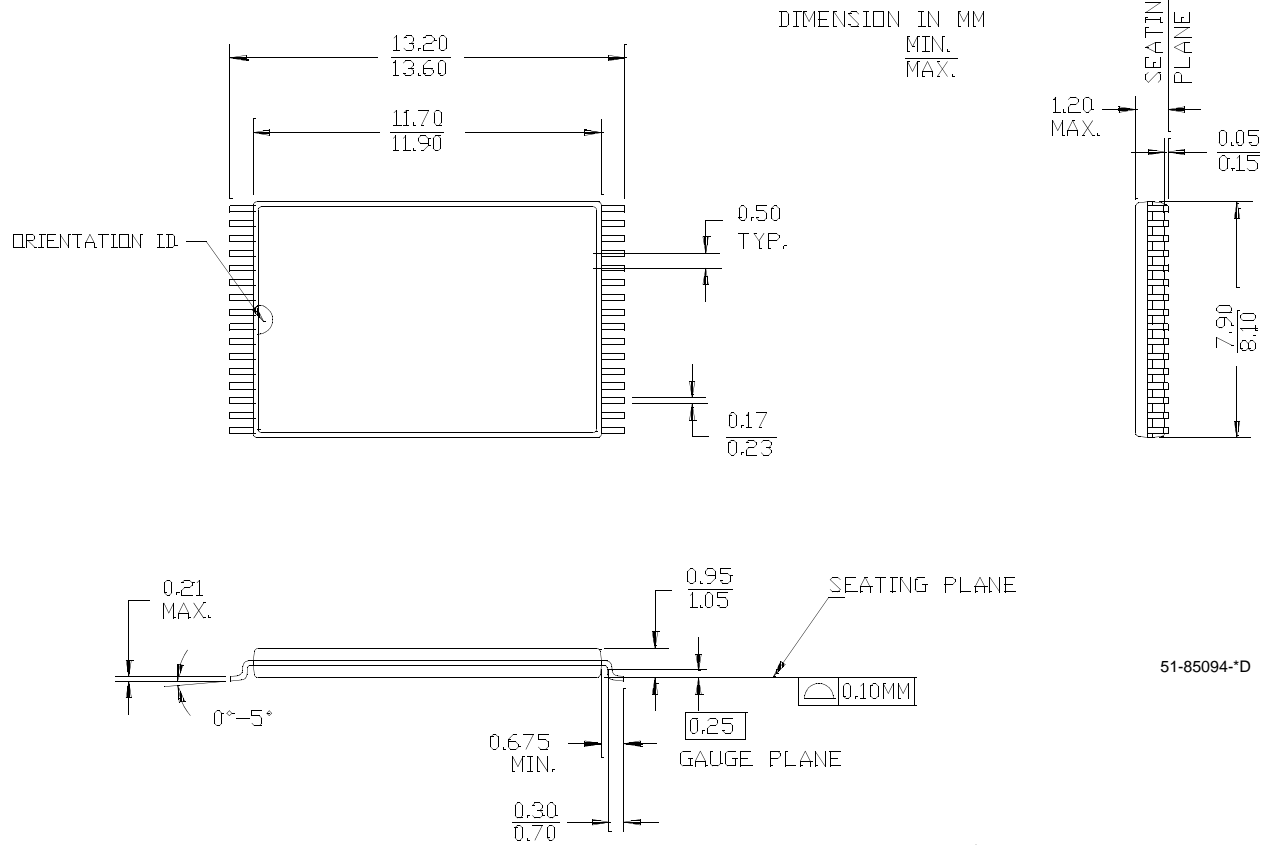
32-pin (450 Mil) Molded SOIC (51-85081)



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**Package Diagrams (continued)**

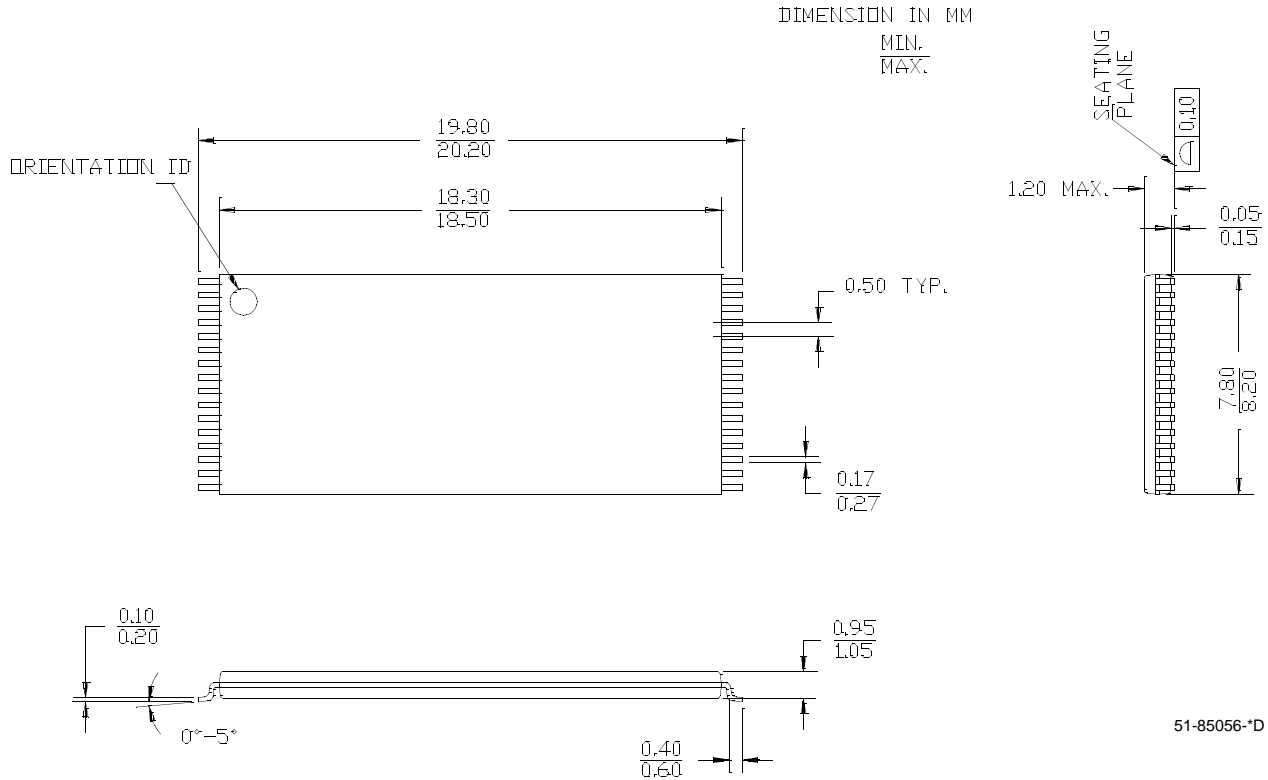
**32-pin STSOP (8 x 13.4 mm) (51-85094)**



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Package Diagrams (continued)

**32-pin TSOP Type I (8 x 20 mm) (51-85056)**



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**Document History Page**

<b>Document Title: CY62128BN MoBL® 1-Mbit (128K x 8) Static RAM</b>				
<b>Document Number: 001-06498</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	426503	See ECN	NXR	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Removed RTSOP Package Updated ordering Information table

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